ZAGORIN O'BRIEN GRAHAM LLP
Intellectual Property Attorneys
7600B N. CAPITAL OF TEXAS HWY, SUITE 350
AUSTIN, TEXAS 78731

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To:	Examiner Michael J. Yigdall	**Fax No.:** **Phone No.:**	(571) 273-3707 (571) 272-3707
Date:	October 28, 2005	**Pages:**	4 (including this sheet)
From:	Steven R. Gilliam	**Sender's Phone No.:** **Sender's Fax No.:**	512-338-6300 512-338-6301

REGARDING:

Title:	AGGRESSIVE PREFETCH OF ADDRESS CHAINS		
Application No.:	09/996,088	**Filed:**	November 28, 2001
Examiner:	Yigdall, Michael J.	**Group Art Unit:**	2192
Atty. Docket No.:	004-7044	**Confirmation No.:**	2526

Please see attached document.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Peter C. Damron et al.		
Title:	AGGRESSIVE PREFETCH OF ADDRESS CHAINS		
Application No.:	09/996,088	Filed:	November 28, 2001
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DRAFT AMENDMENT

1. In a scheduler for computer code, which is encoded in one or more computer readable media, wherein certain operations are likely to stall execution of the computer code and thereby provide latency for completion of one or more pre-executable operations, a method of scheduling certain of the operations, the method comprising:

for one or more sequences of operations that follow a speculation boundary and that define respective dependency chains, including pre-executable operations, which lead to likely stalls, representing speculative copies thereof as duplicate chains; and

scheduling operations of the computer code, wherein the scheduling of operations from the duplicate chains is performed without regard to dependence of respective original operations on the speculation boundary, thereby scheduling certain of the operations above the speculation boundary into position preceding at least one of the operations likely to stall execution of the computer code,

wherein the speculation boundary corresponds to an operation upon which the respective original operations depend.

13. A computer implemented method of hiding latency in computer code wherein certain operations thereof are likely to stall execution, the method comprising:

identifying sequences of operations that define respective original dependency chains that lead to likely stalls and for at least some of the identified sequences, representing duplicate dependency chains thereof; and

scheduling at least some operations from the duplicate dependency chains above at least one of the likely-to-stall operations,

wherein the operations scheduled from the duplicate dependency chains are scheduled above a speculation boundary that corresponds to an operation upon which the original dependency chains depend and that precedes the at least some of the identified sequences.

37. A computer implemented method of making a computer program product that encodes program code for which memory access latency is at least partially hidden on execution thereof, the method comprising:

for operations that form addressing chains that lead to a likely cache miss, representing speculative copies thereof; and

scheduling the speculative copies without regard to a corresponding speculation boundary, wherein operations of the speculative copies are scheduled above the corresponding speculation boundary and above a preceding operation that is likely to stall,

wherein the speculation boundary, which precedes the operations that form addressing chains, corresponds to an operation upon which the operations that form addressing chains depend.

47. An apparatus comprising:

a code preparation facility for transforming schedulable code into scheduled code; and

means for scheduling speculative copies of operations that form dependency chains that lead to a likely stall, the scheduling placing the speculative operations above a preceding at least one other operation that is itself

likely to stall, thereby hiding in the scheduled code latency of the speculative operations,

wherein the scheduling also places the speculative operations above a speculation boundary that precedes the operations that form the dependency chains,

wherein the speculation boundary corresponds to an operation upon which the operations that form the dependency chains are dependent.